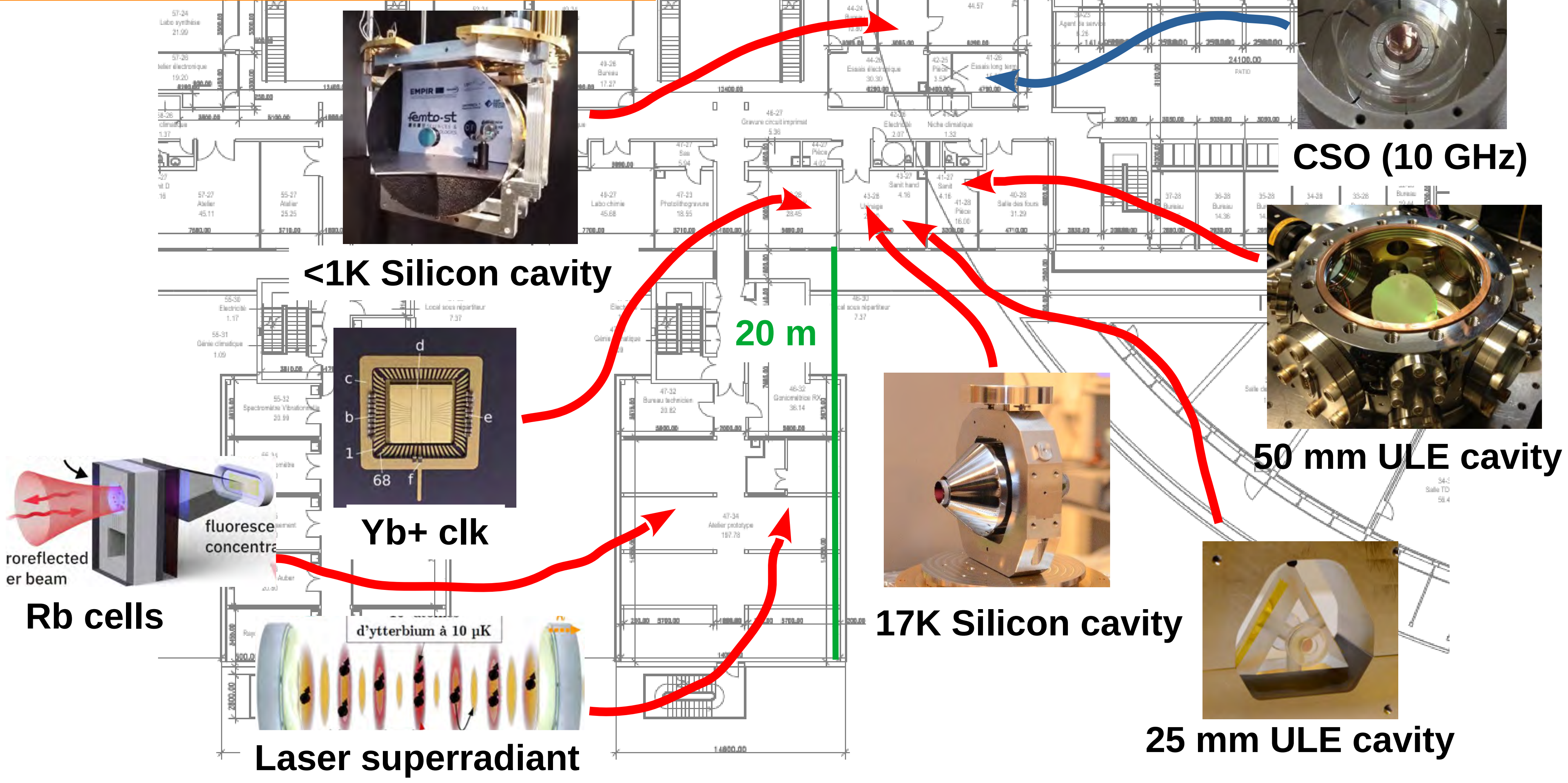
Local distribution of optical references based on digital electronic PLL

Martina Matusko, Shambo Mukherjee, Ivan Ryger, Séverine Denis, Gwenhaël Goavec-Merou, Jacques Millo, Remi Meyer, Clément Lacroûte, Émile Carry, Jean-Michel Friedt,Marion Delehaye

AG Refimeve, LPL, le 03/10/2024

Local context



Outline

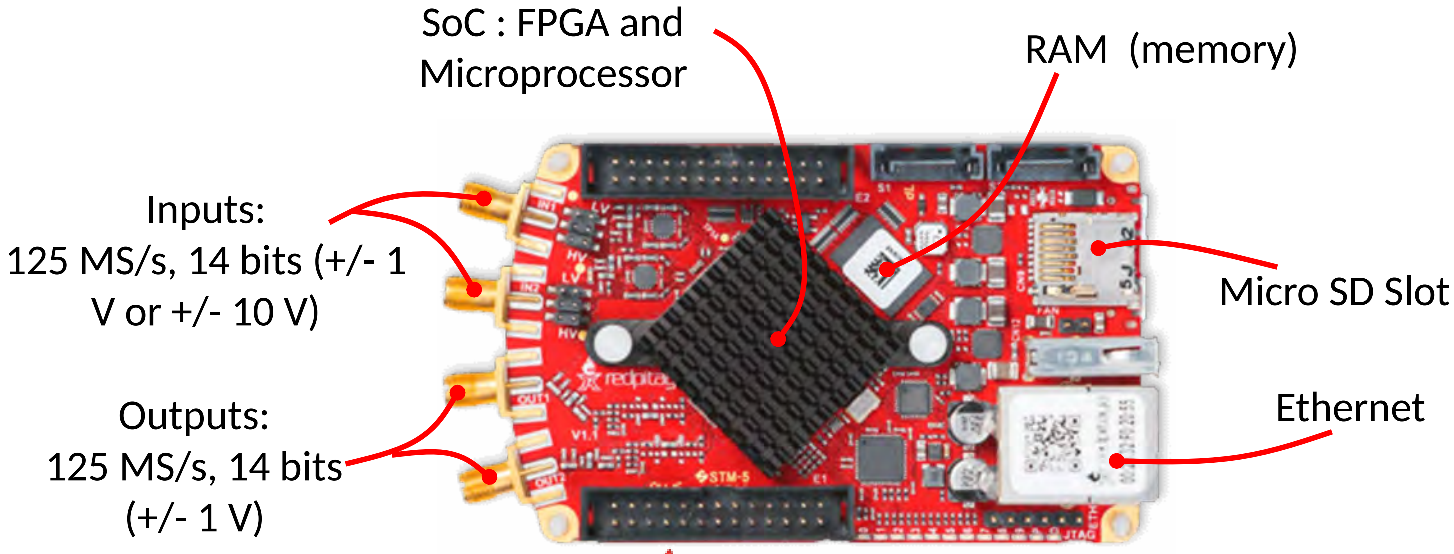
- Red Pitaya Platform (FPGA)
- Link stabilization with Red Pitaya
- Link stabilization with undersampling technic
- Others applications

Red Pitaya Platform

STEMLab 125-14

FPGA (Field-Programmable Gate Array):

- logic functions
- Multipliers (48 bits)
- Memory RAM
- DMA (CPU-FPGA data transfert)
- LookUp tables (LUT)



redpitaya

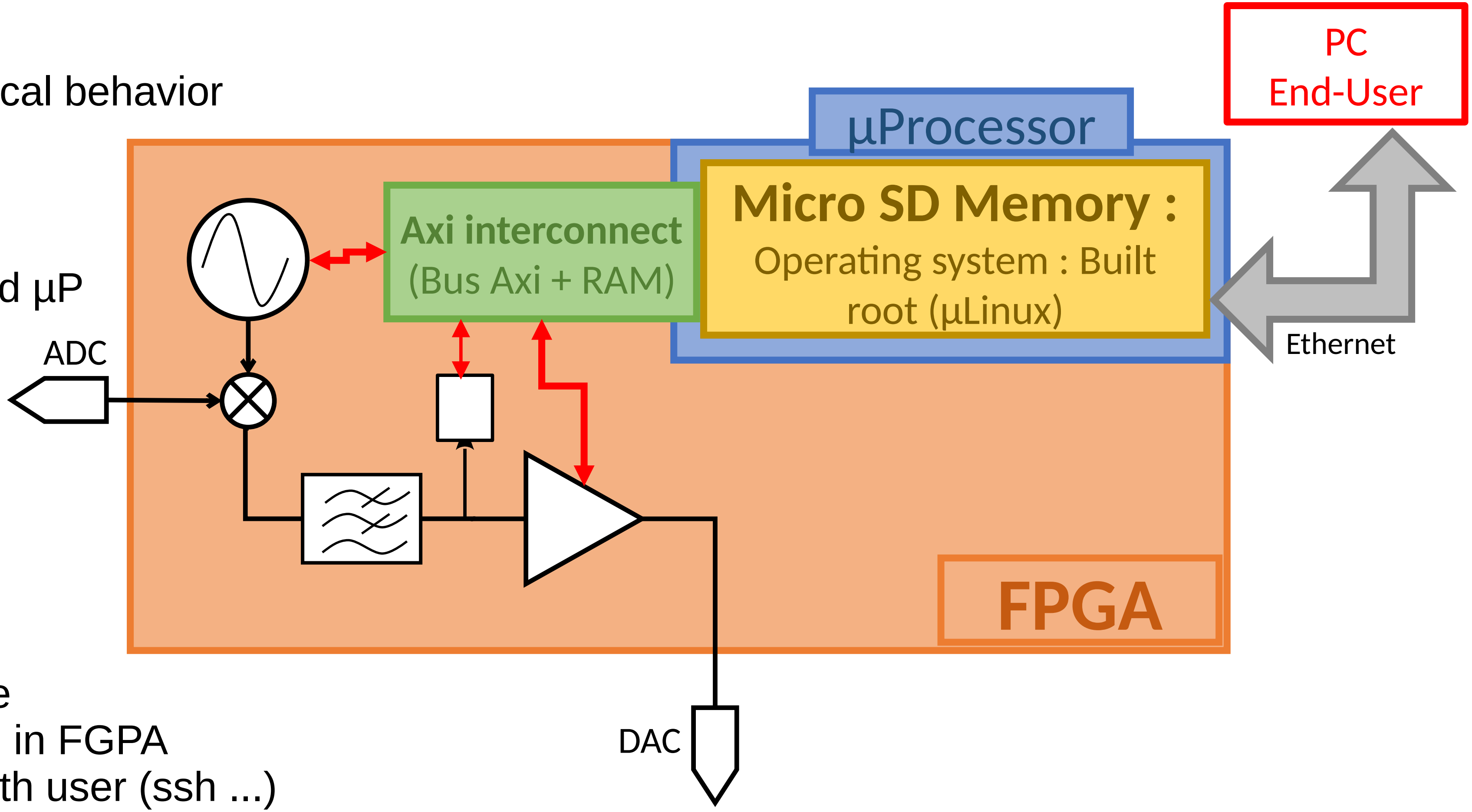
- *CPU*: Dual-Core ARM Cortex-A9 MPCore
- *FPGA*: Xilinx Zynq 7010

Red Pitaya Platform

overview

FPGA:
Configured for logical behavior

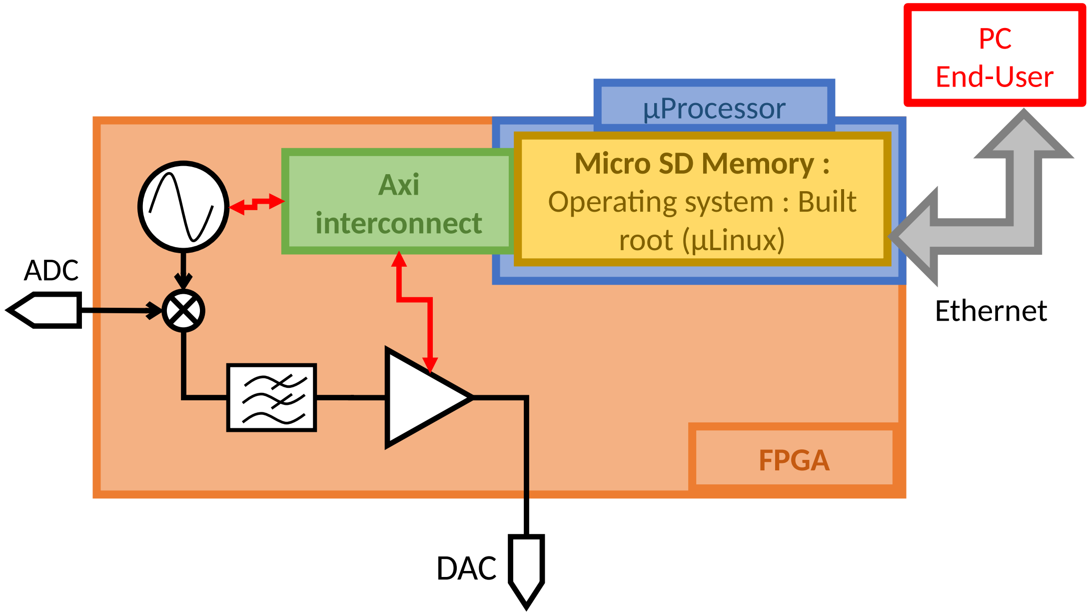
AXi interconnect:
Communication
between FPGA and µP



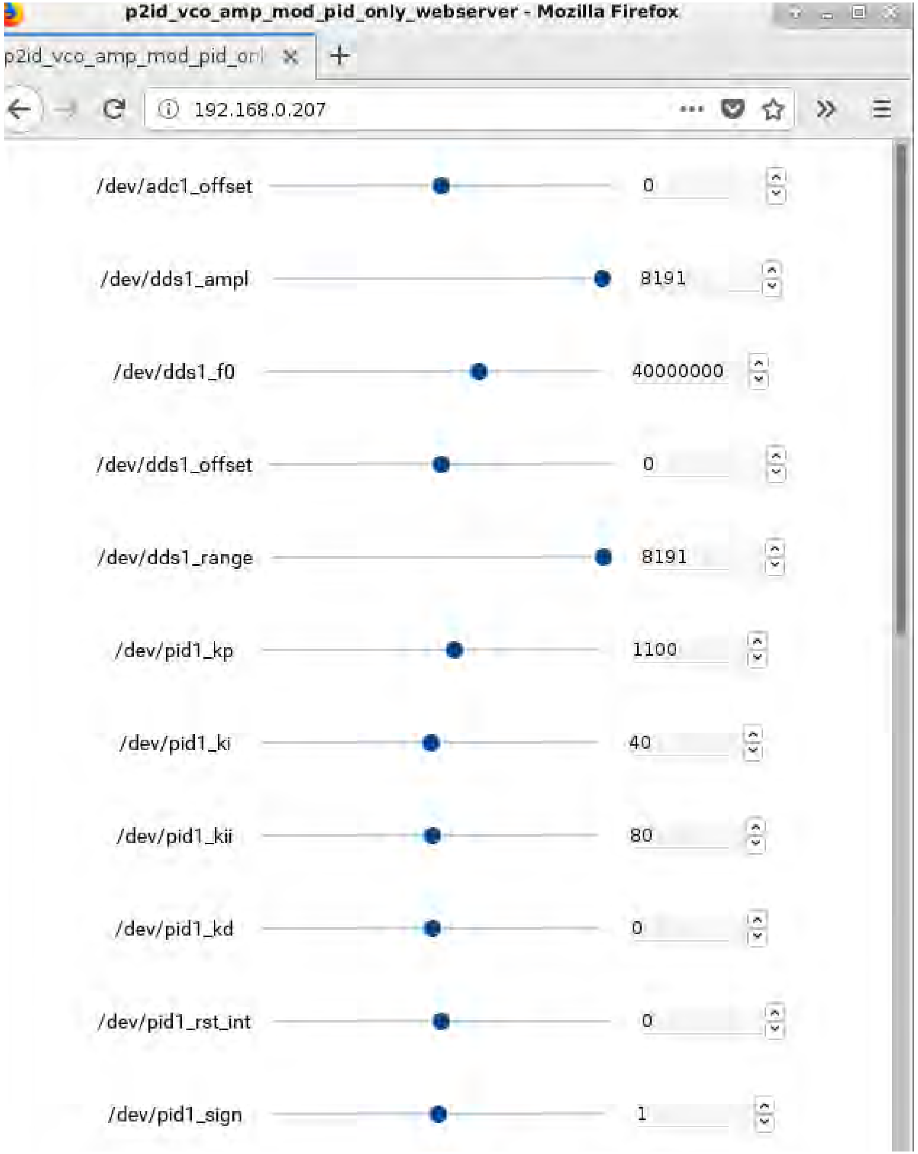
µProcessor:
High level software
set/get information in FGPA
Communication with user (ssh ...)

Red Pitaya Platform

User interface



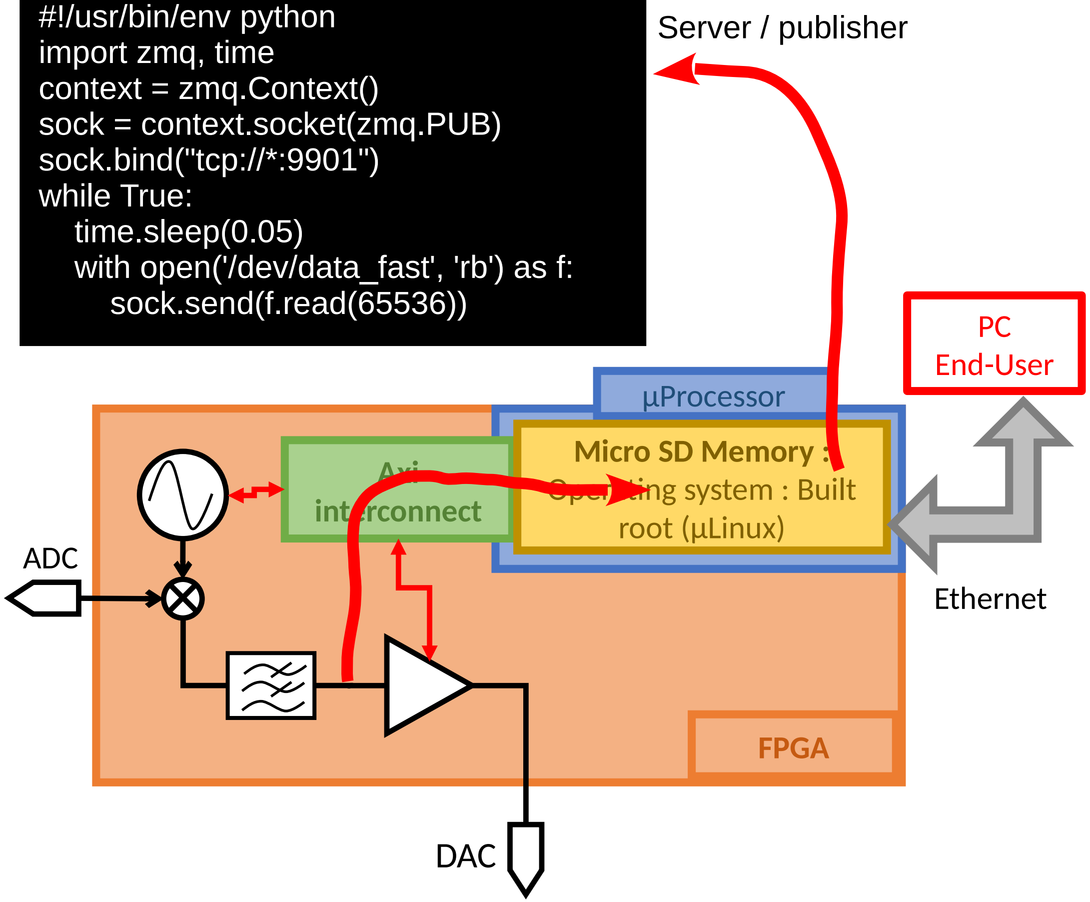
liboscimp_fpga.shifter_set("/dev/shifterDyn_1", int(value))



Red Pitaya Platform

Signal monitoring

```
#!/usr/bin/env python
import zmq, time
context = zmq.Context()
sock = context.socket(zmq.PUB)
sock.bind("tcp://*:9901")
while True:
    time.sleep(0.05)
    with open('/dev/data_fast', 'rb') as f:
        sock.send(f.read(65536))
```



Red Pitaya Platform

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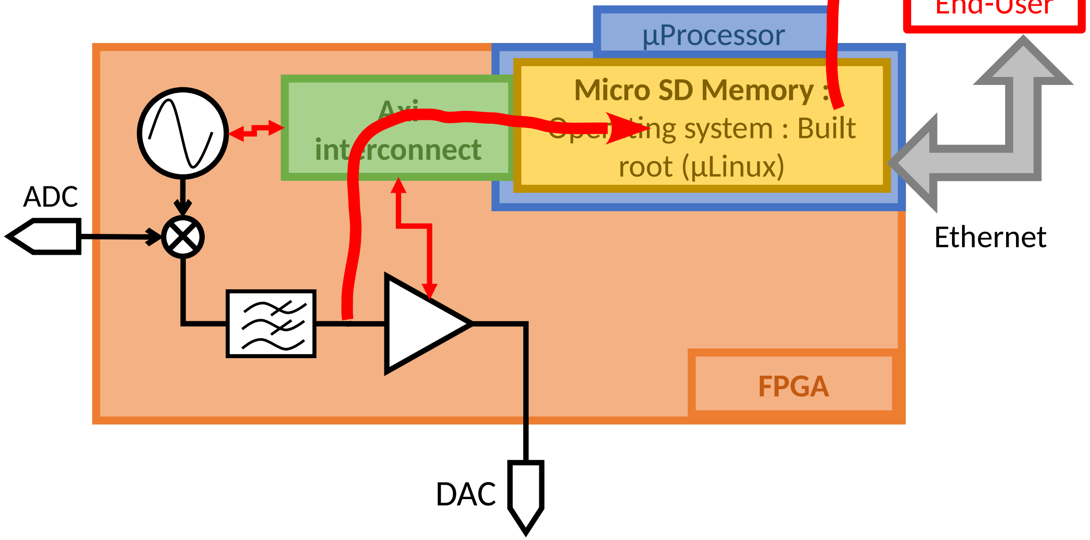
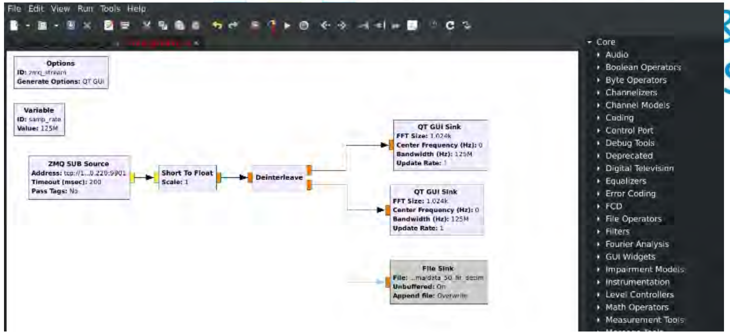
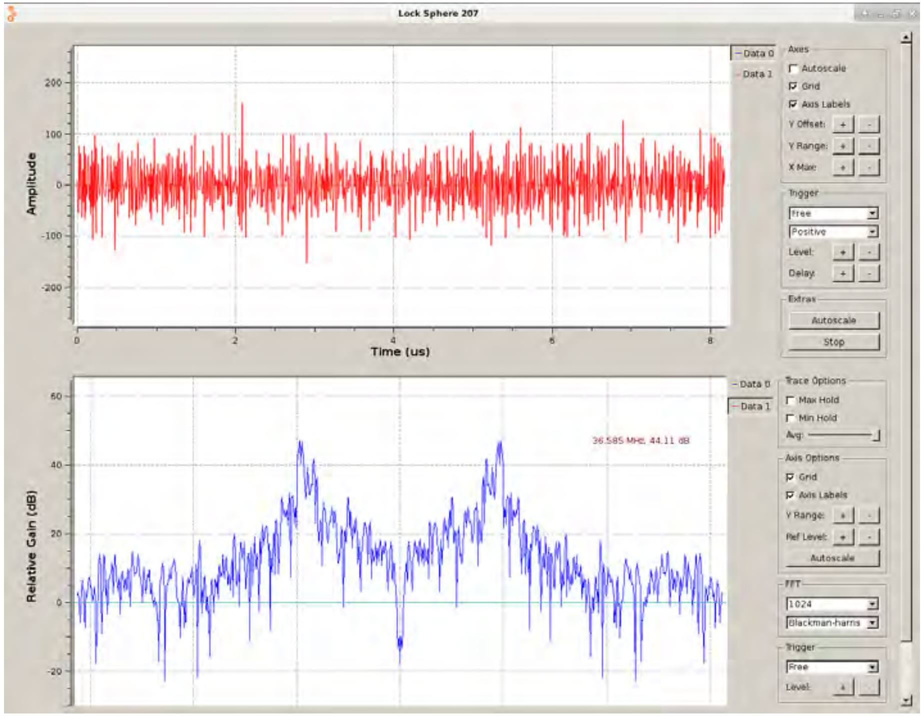
```

Server / publisher

Client / Subscriber







Red Pitaya Platform

Software “suite”

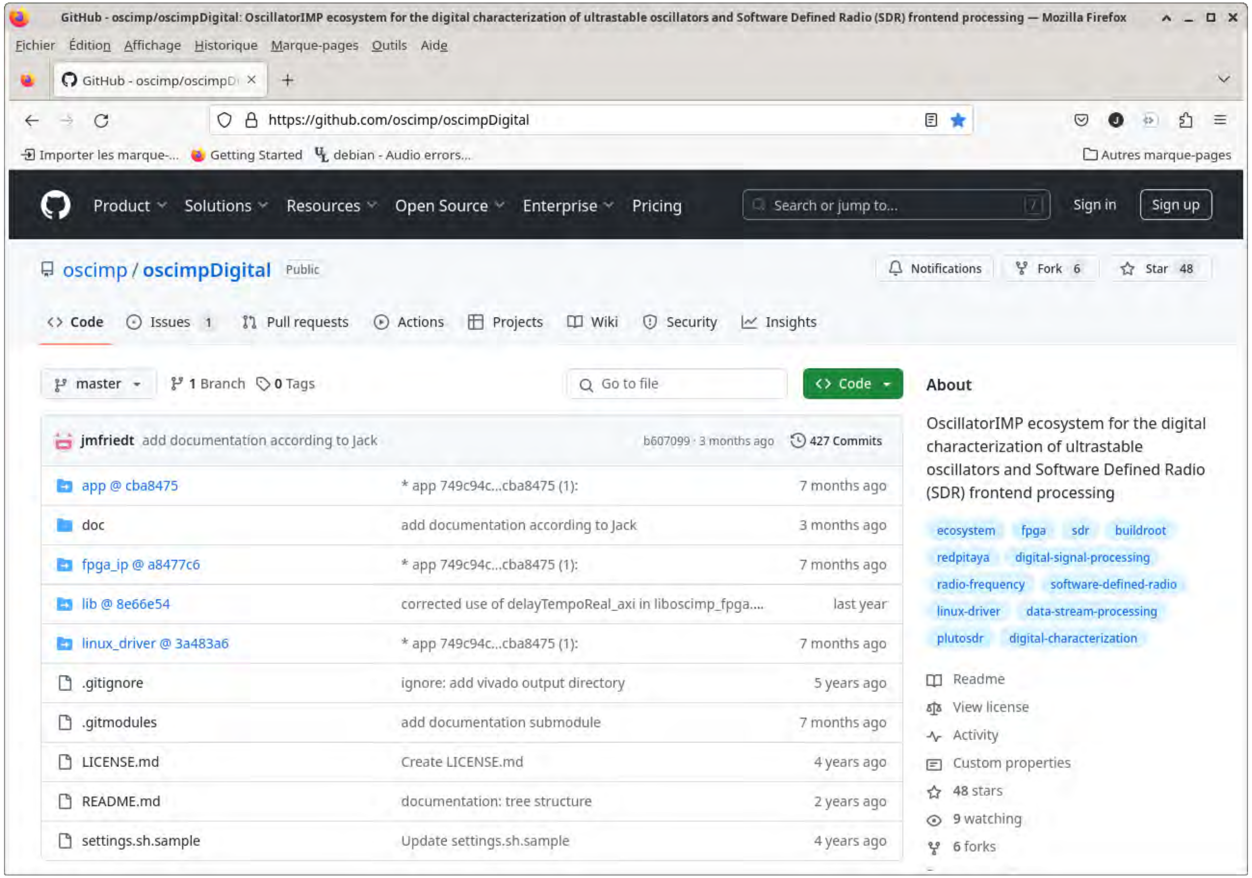
https://github.com/oscimp/oscimpDigital

Open software

Available for few eval boards

Tutorial available

… but not so easy



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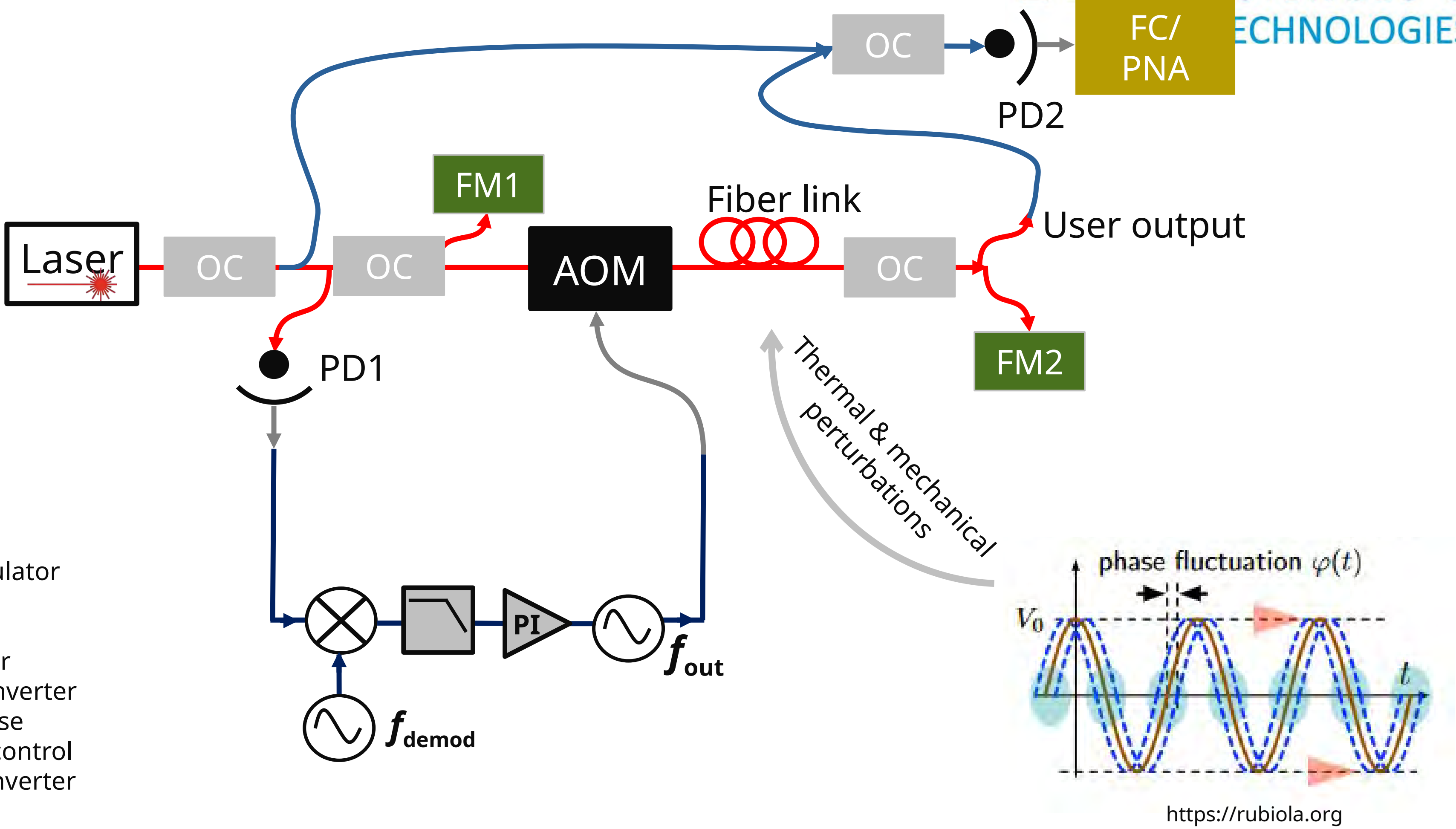
- Link stabilization with undersampling technic
- Others applications

Fiber link stabilization

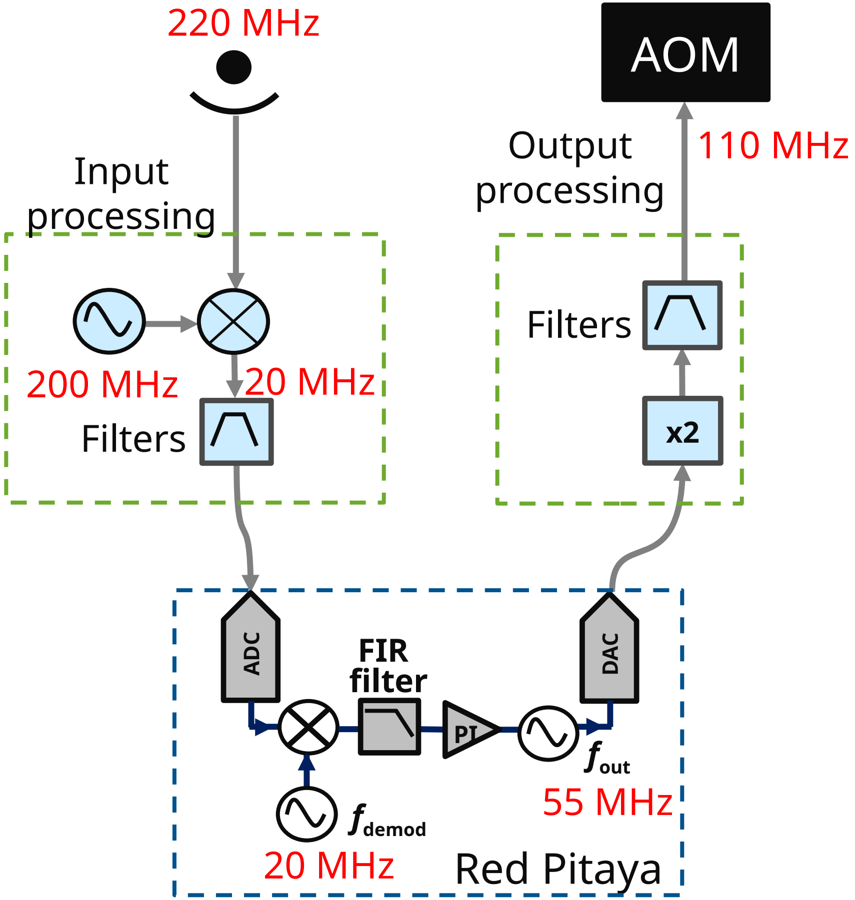
Concept

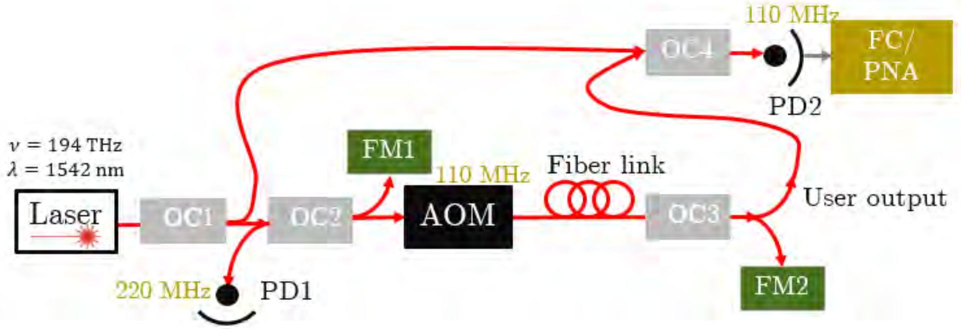


OC: optical coupler
FM: Faraday mirror
AOM: acousto-optic modulator
PD: photodiode
FC: frequency counter
PNA: phase-noise analyzer
ADC: analog-to-digital converter
FIR: finite impulse response
PI: proportional-integral control
DAC: digital-to-analog converter

Fiber link

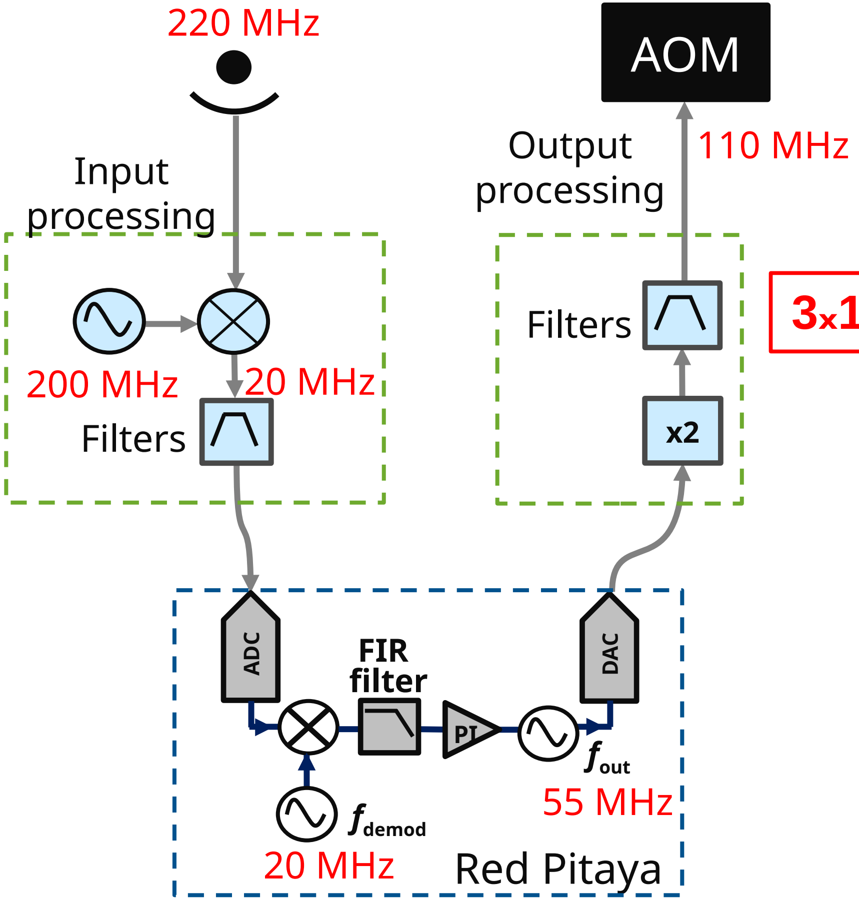
Red Pitaya

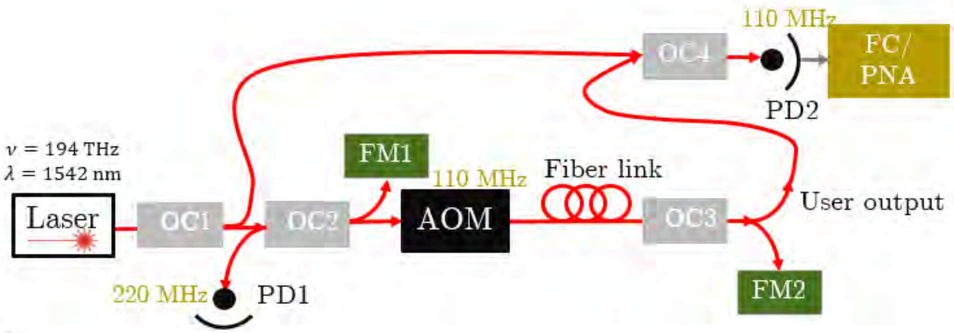


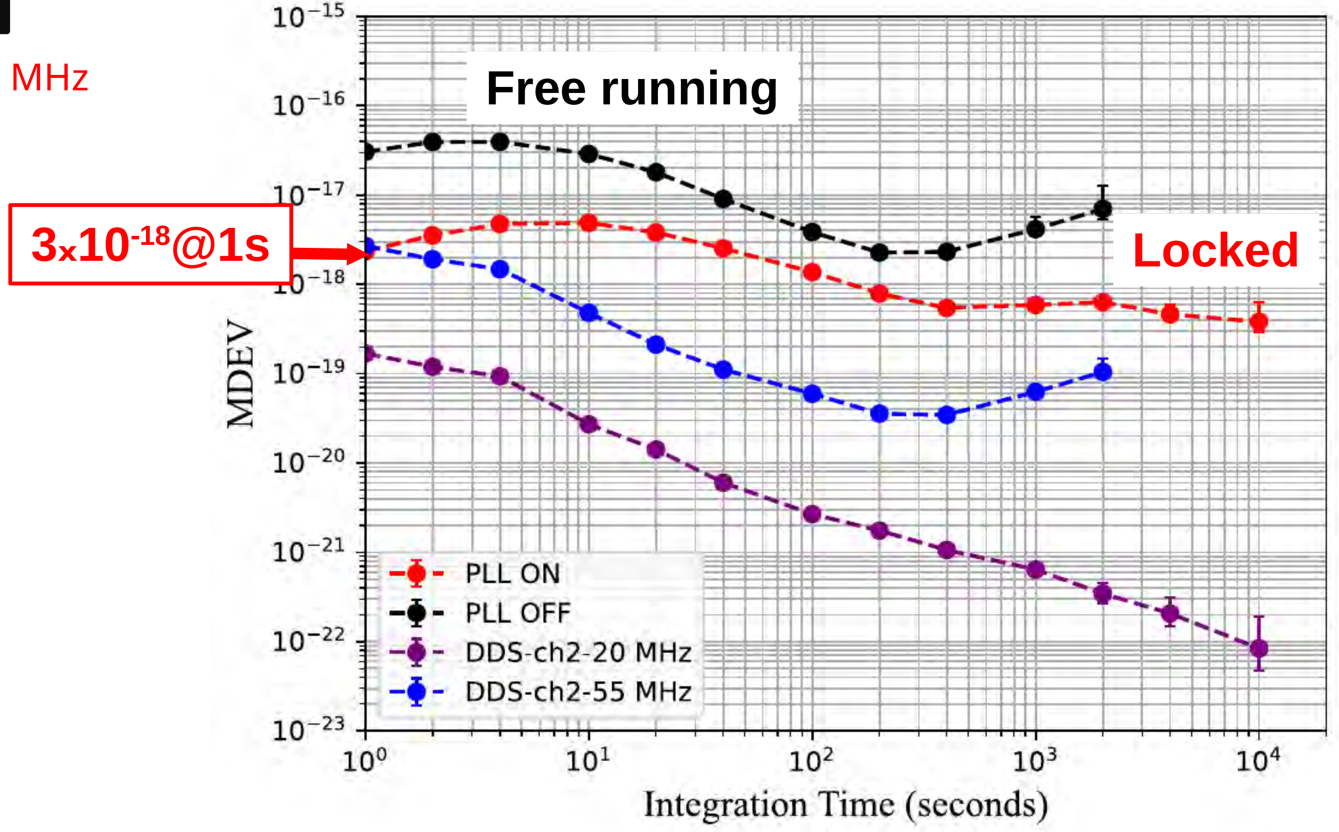


Fiber link

Red Pitaya

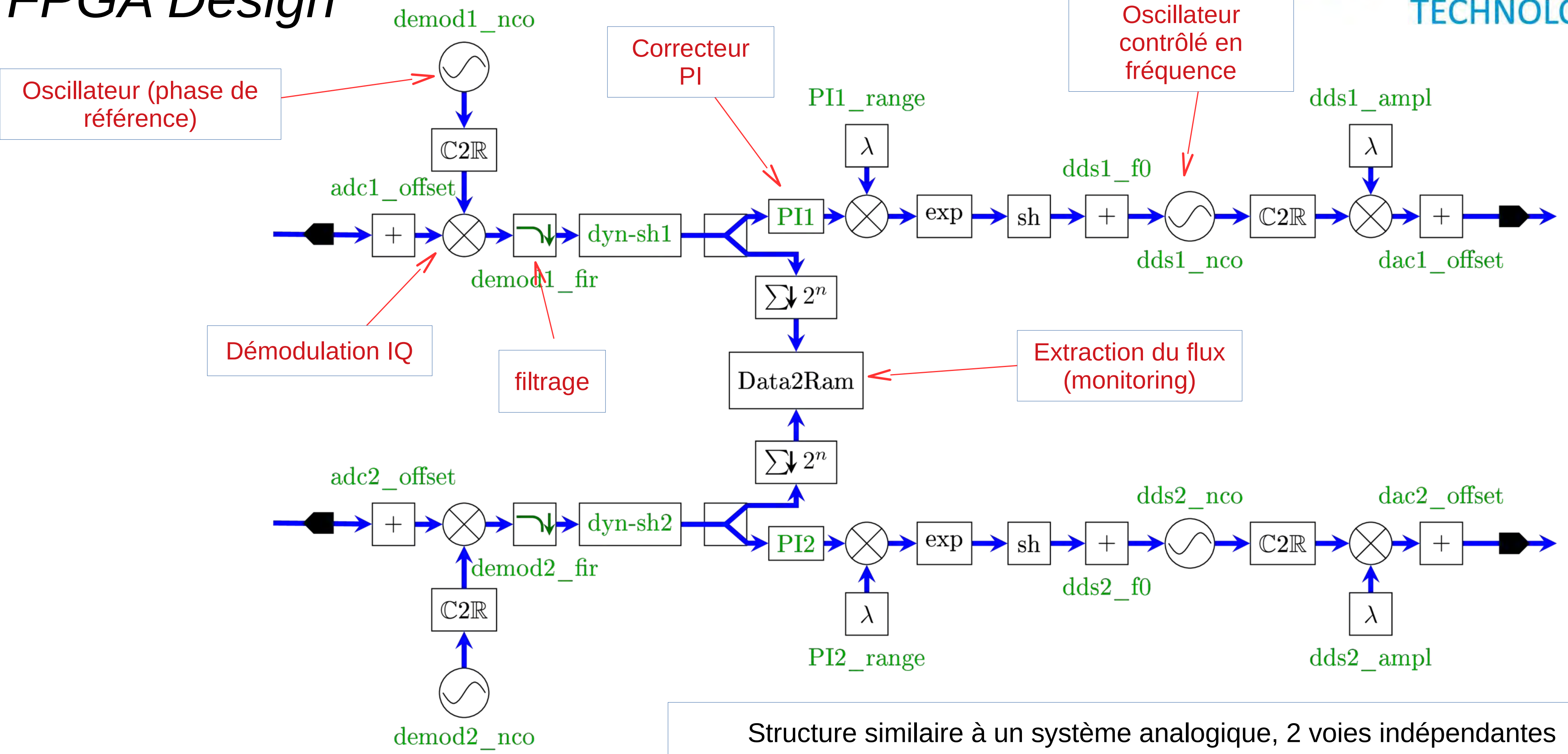






Fiber link

FPGA Design



Structure similaire à un système analogique, 2 voies indépendantes

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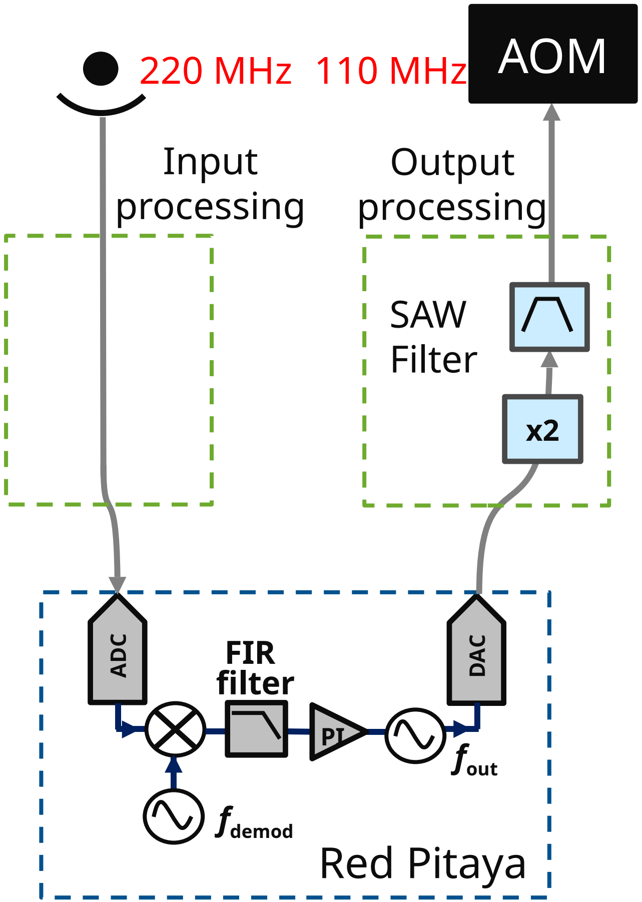
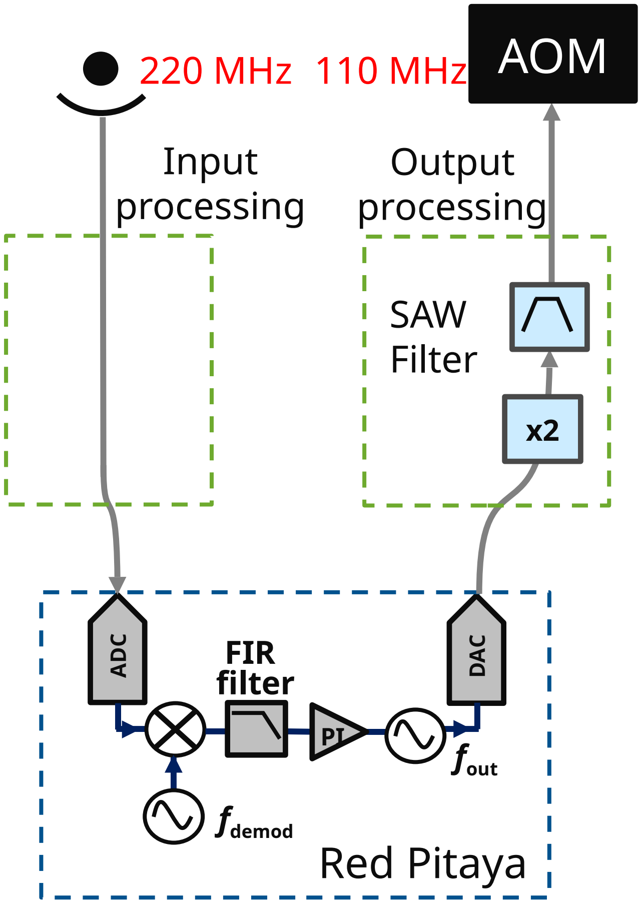
Undersampling - 1

STEMlab 125-14

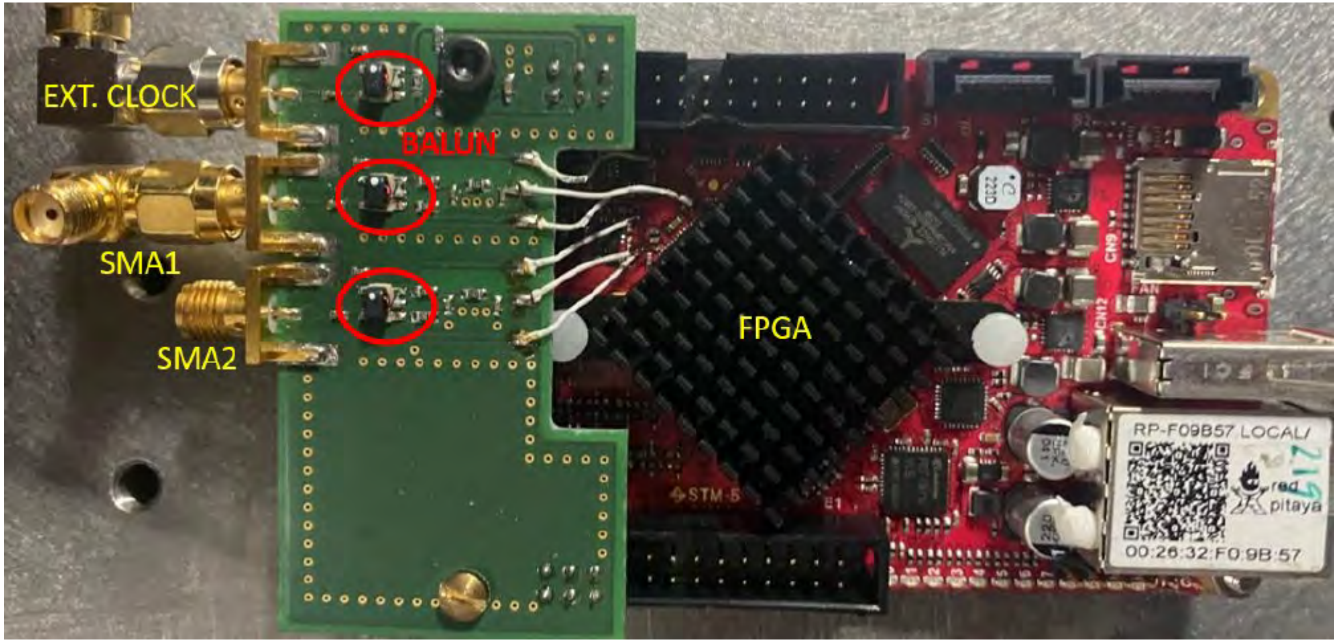


Undersampling - 1

STEMlab 125-14



Bypass anti-aliasing filters
Connect external clock
« extension board » (balun / differential input)



Fiber link

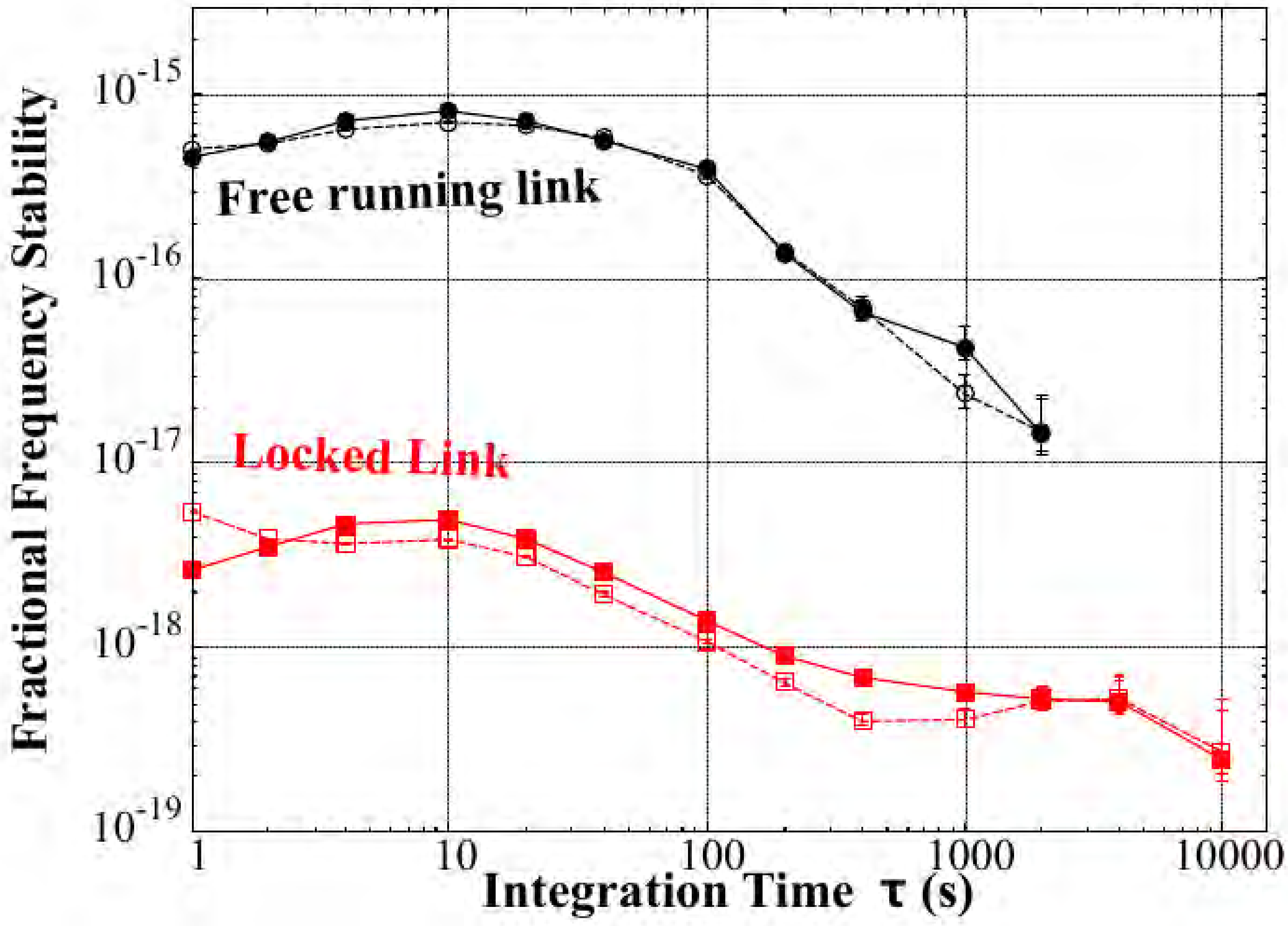
Performances

□ **Undersampling**

4_x10^{-18}@1s

■ **Red Pitaya (regular)**

3_x10^{-18}@1s



Undersampling

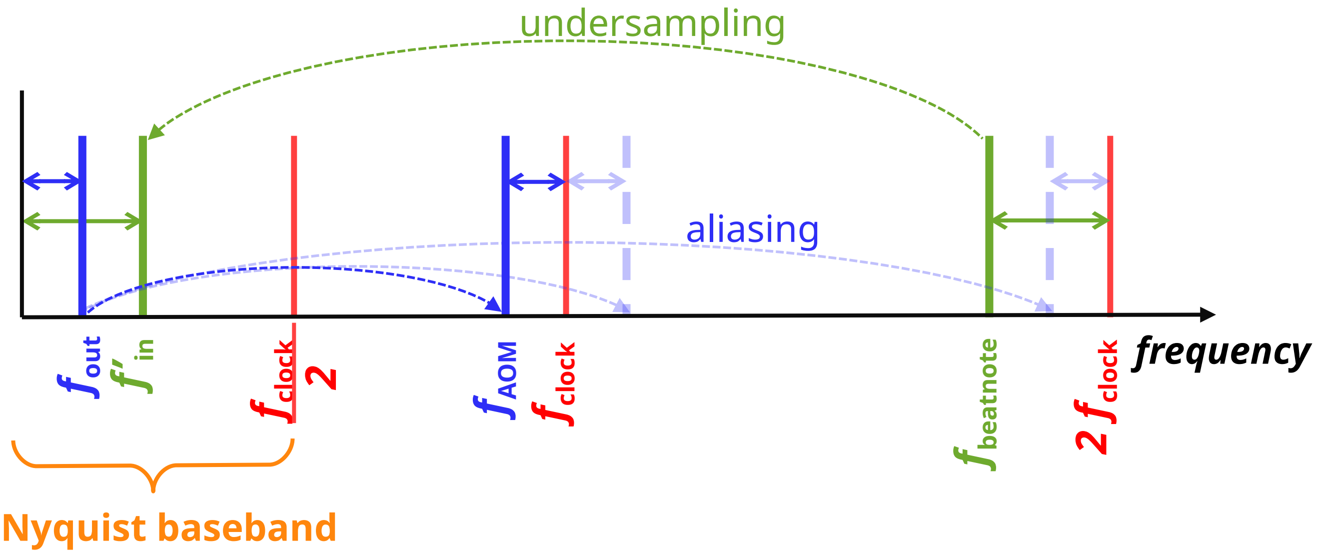
Principle

signal at ADC

signal at DAC

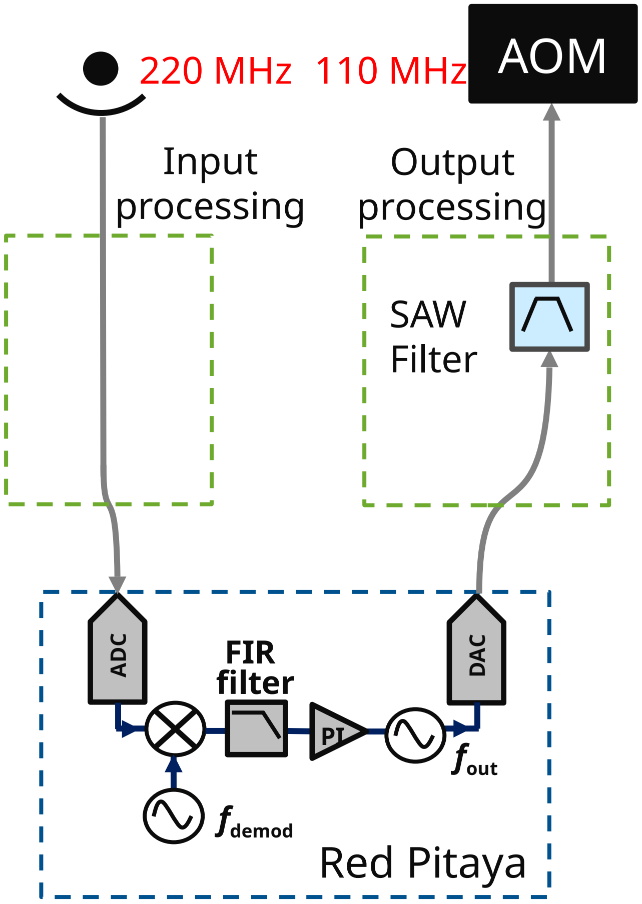
Nyquist: $f'_{in} = |f_{in} - n \times f_{clock}|,\ 0 < f'_{in} < f_{clock}/2$

Aliasing: $n \times f_{clock} \pm f_{out}$



Undersampling - 2

SDRlab 122-16

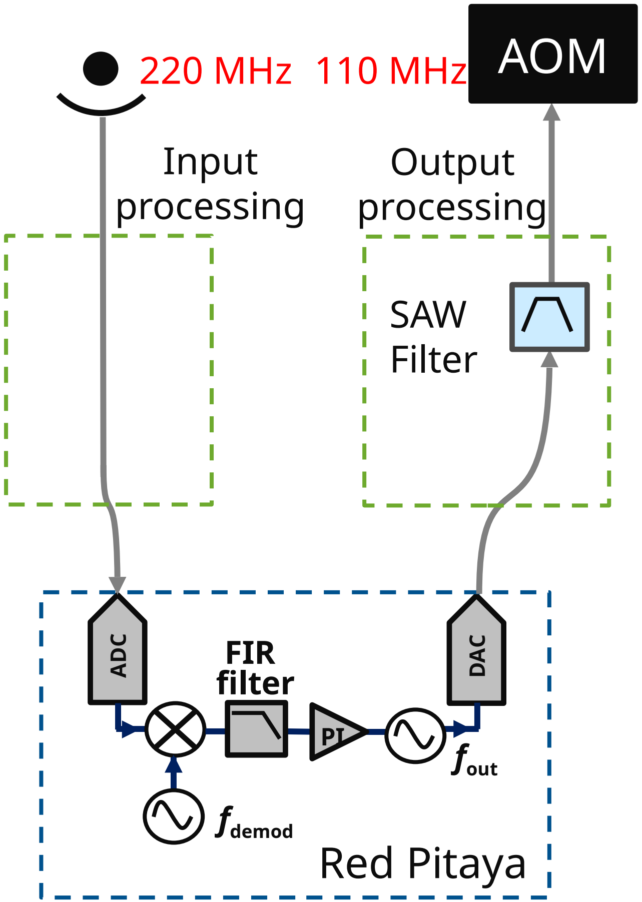


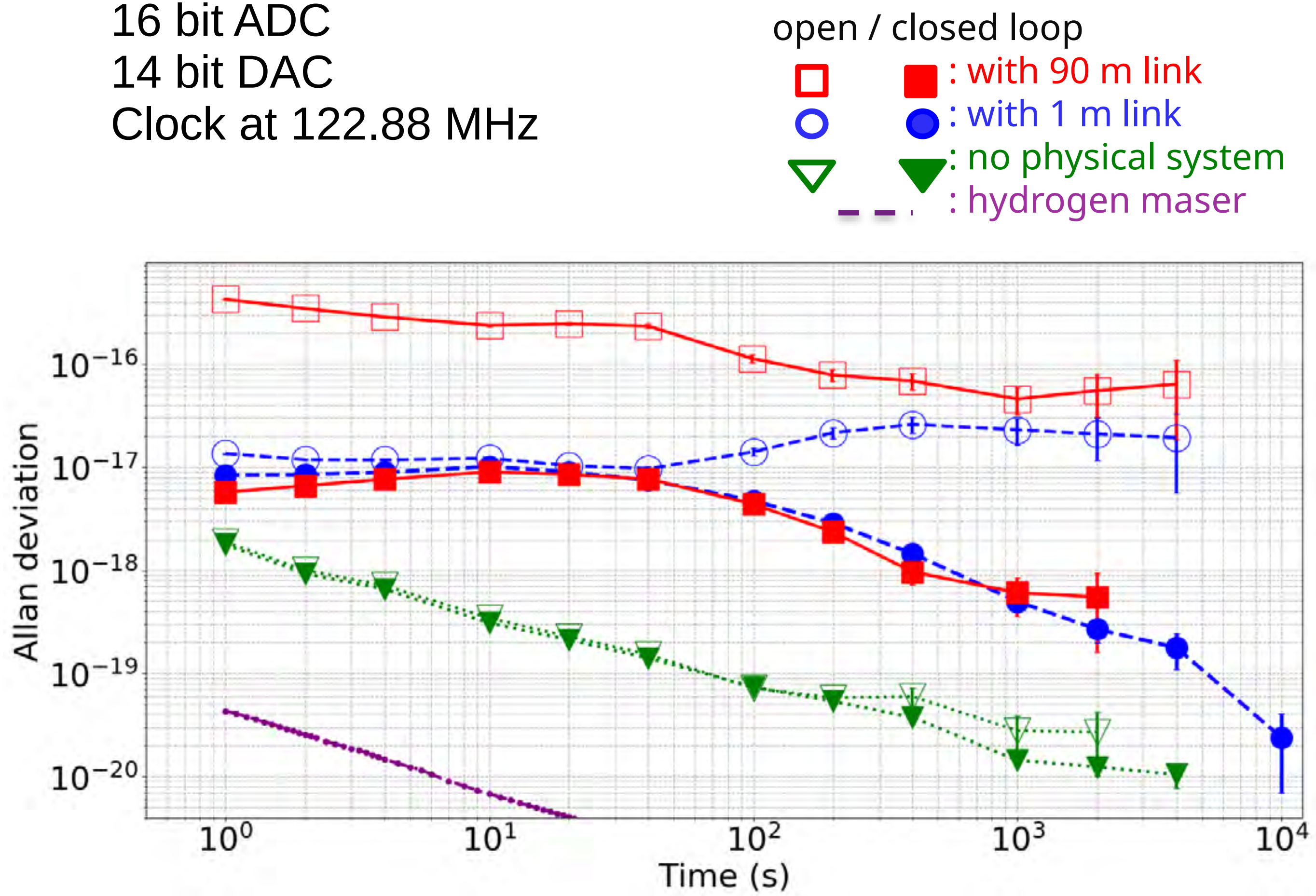
No anti-aliasing filters
16 bit ADC
14 bit DAC
Clock at 122.88 MHz

Undersampling - 2

SDRlab 122-16

No anti-aliasing filters
16 bit ADC
14 bit DAC
Clock at 122.88 MHz





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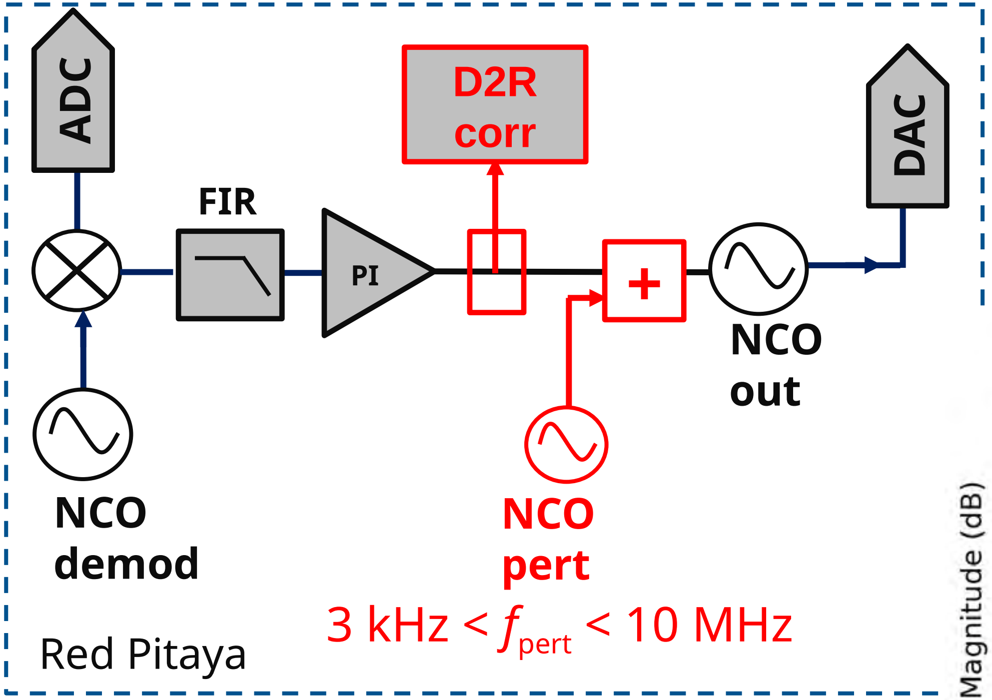
PLL characterization

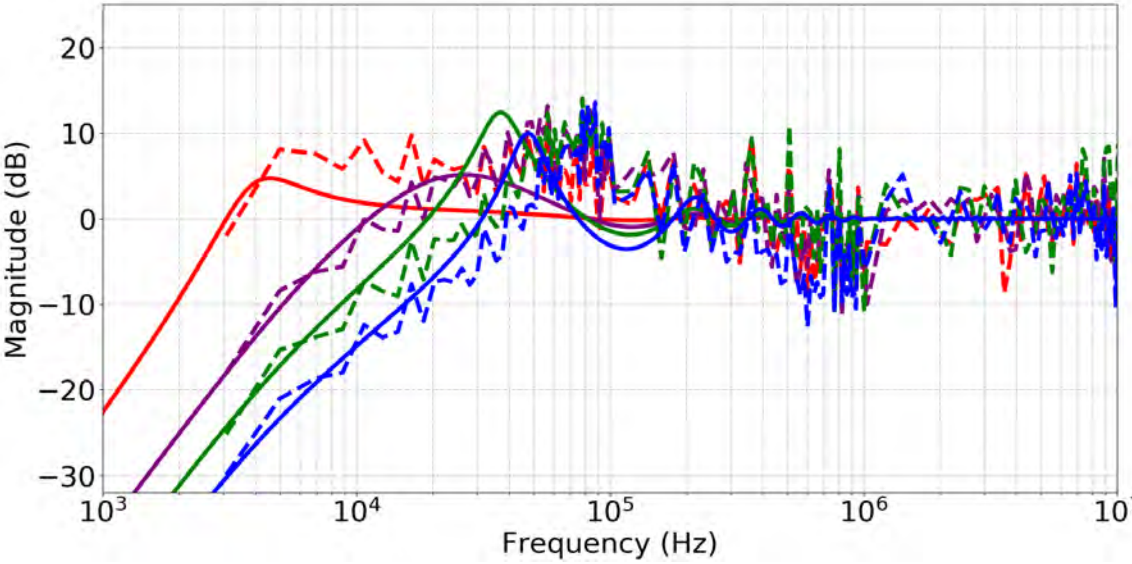
Tune PI gain



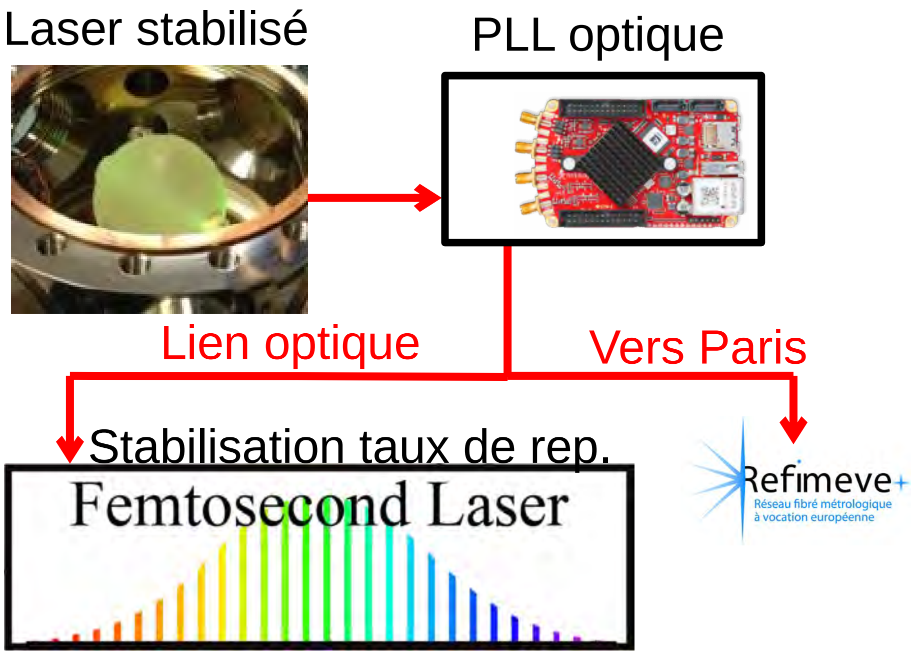
Red Pitaya adapted design

D2R: data-to-ram acquisition, NCO: numerically cor
oscillator. FIR: finite impulse response filter.

Red curves: lowest PI gains,
purple curves: 5×red-,
green curves: 10×red-,
blue: 20×red-curve PI gains



Application à la suppression de dérive de cavité



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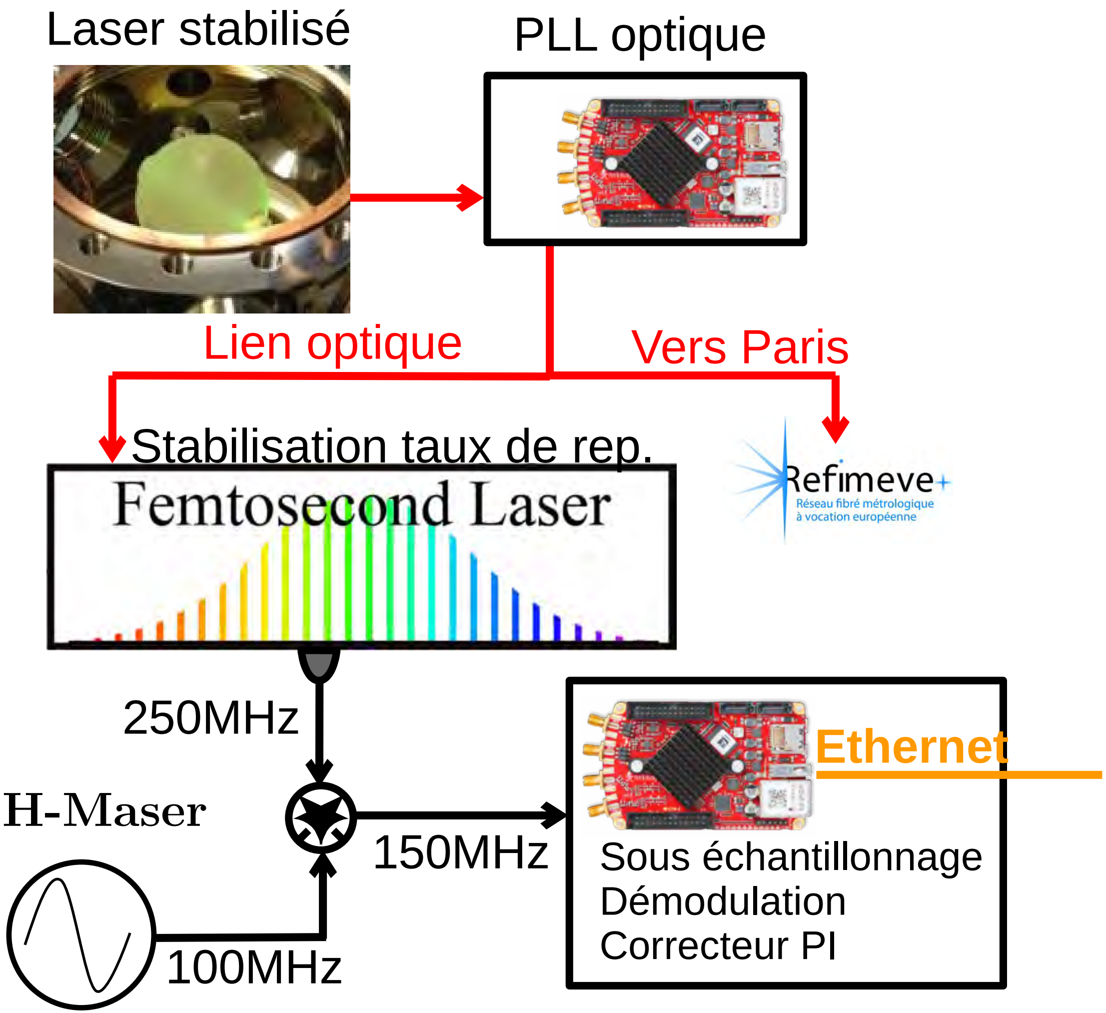

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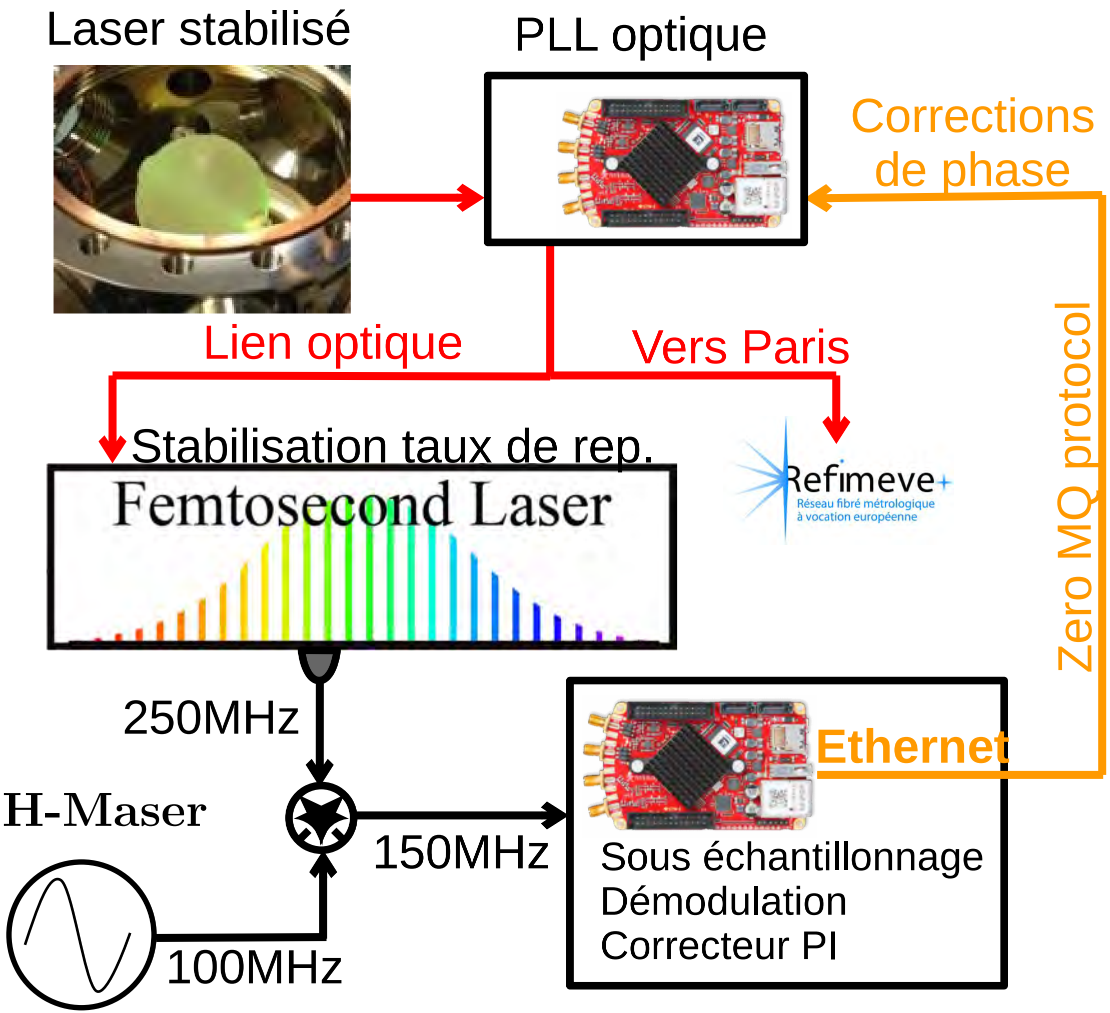

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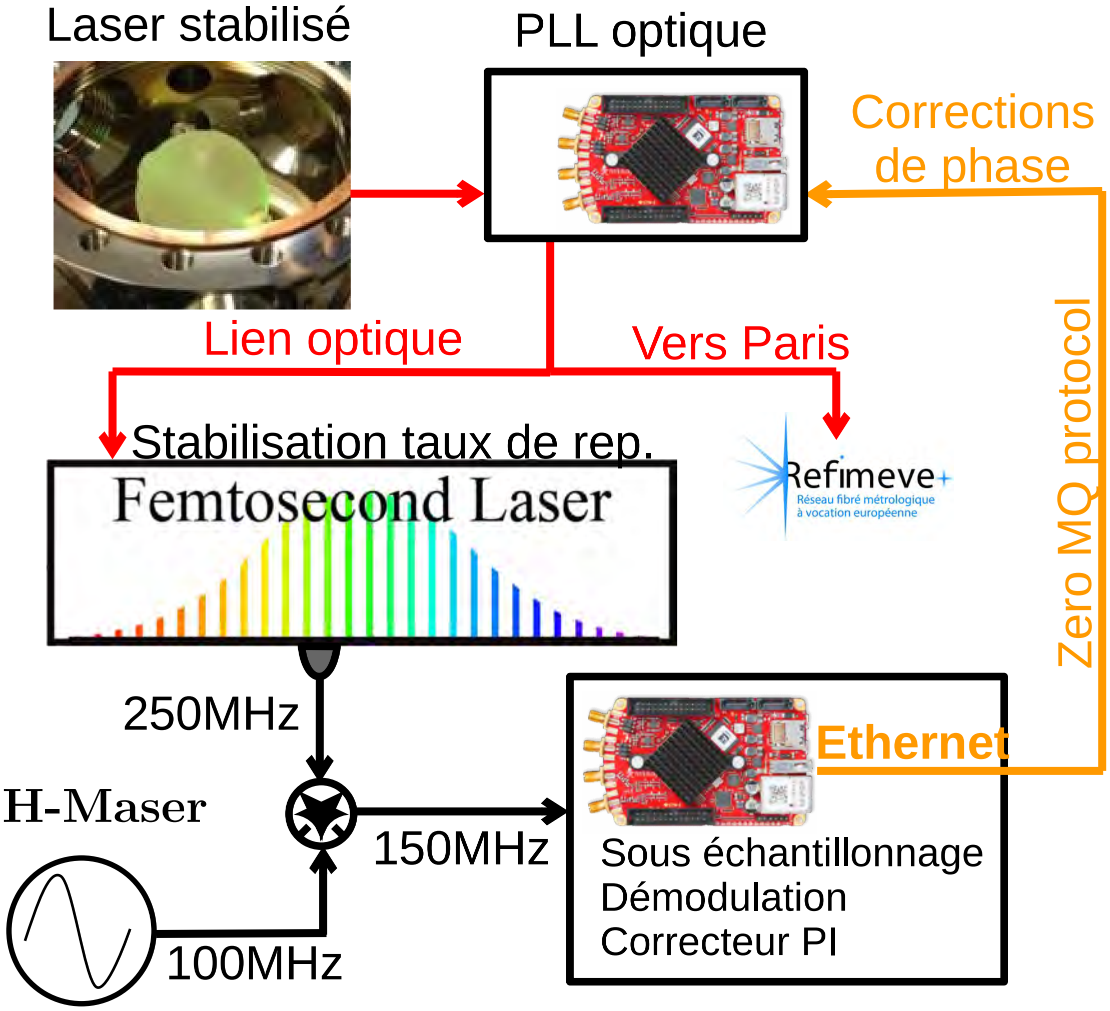
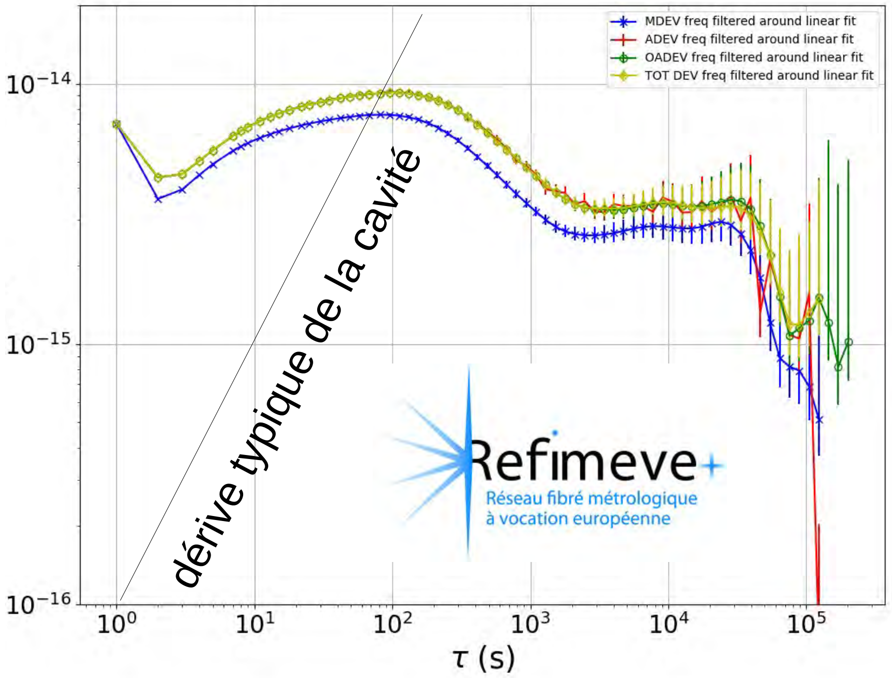
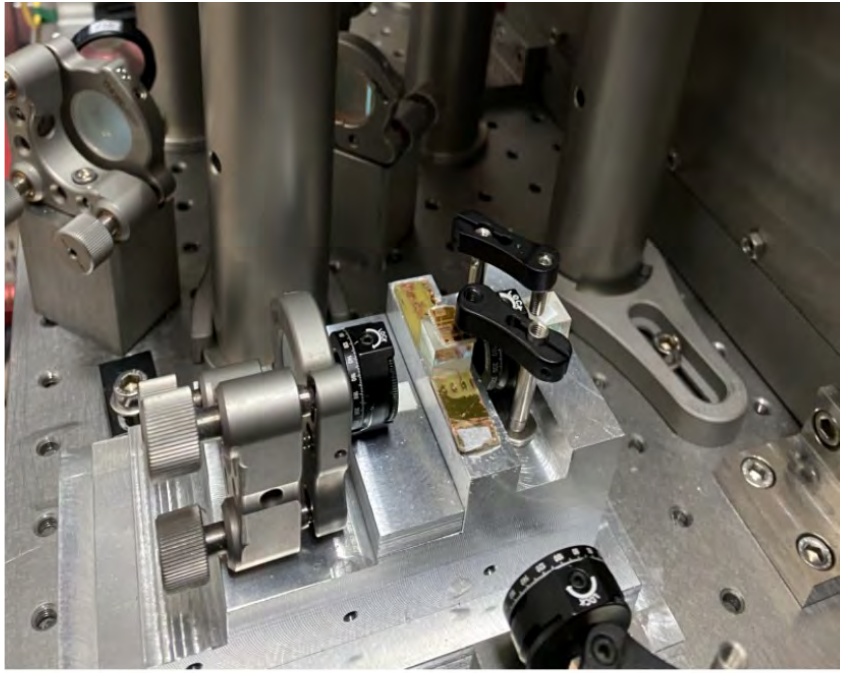


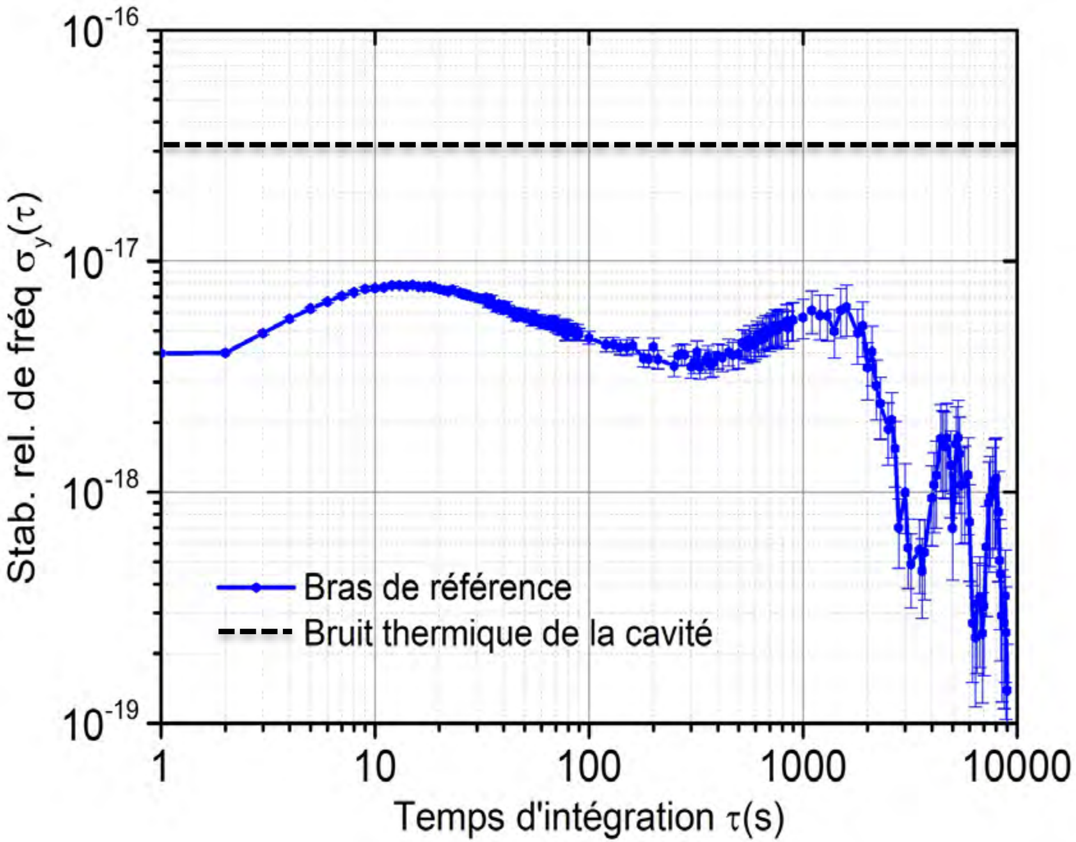
Comparaison SYRTE – FEMTO-ST



Free space ref arm

Characterization



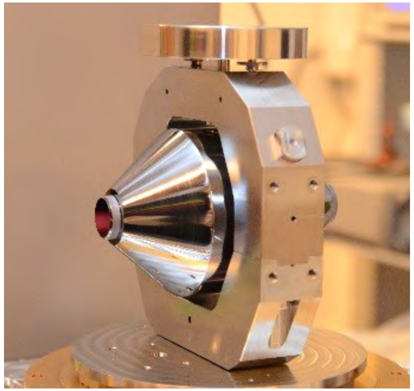


Conclusions

Link stabilization below 10^{-17} ==> compatible with our needs (silicon cryo cavity)

Software « suite » open : *oscimpDigital* in *github*

FPGA also used for PDH lock, Phase detection, RAM stabilization, apply sequences in CPT clock ...



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